AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

What is claimed is:

1. (Currently Amended) A device for generating a random sequence of bits comprising:

oscillating means having an input terminal for receiving a bias as input, the oscillating means comprising at least one oscillator amplifier;

amplifying means comprising each the at least one oscillator amplifier and a corresponding at least one differential amplifier coupled to each the at least one oscillator amplifier;

a load further comprising cascoded transistors coupled to the amplifying means and a power supply; the load being adapted to protect the amplifying means from interfering signals; and

a tail current source coupled to the amplifying means and grounding means.

2. (Previously Presented) The device according to claim 1, wherein the number of oscillator amplifiers is odd and greater than one, and the oscillator amplifiers are coupled in series.

3. (Previously Presented) The device according to claim 1, wherein the amplifying means further comprises a common-source amplifier.

4. (Previously Presented) The device according to claim 3, wherein the common source amplifier further comprises transistors having a differential topology.

5. (Canceled)

6. (Currently Amended) The device according to claim 1, wherein the ~~load comprises at least one resistor~~ cascoded transistors act as a resistance coupled to the amplifying means.

7. (Previously Presented) The device according to claim 1, further comprising grounding means, wherein the tail-current source is coupled to the amplifying means and the grounding means adapted to provide common-mode feedback.

8. (Currently Amended) The device according to claim 1, wherein the ~~load~~ cascoded transistors, the amplifying means and the tail-current source comprise MOS (Metal Oxide Semiconductor) transistors.

9. (Currently Amended) The device according to claim 1, wherein the ~~load~~ cascoded transistors, the amplifying means and the tail-current source comprise BJT (Bipolar Junction Transistors) transistors.

10. (Currently Amended) The device according to claim 1, wherein the ~~load comprises~~ cascoded transistors comprise PMOS transistors and the amplifying means and the tail-current source comprise NMOS transistors.

11. (Currently Amended) The device according to claim 1, wherein the ~~load comprises~~ cascoded transistors comprise NMOS transistors and the amplifying means and the tail-current source comprise PMOS transistors.

12. (Previously Presented) The device according to claim 11, wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source and the width-over-length ratio of a second transistor pair of the load is at least 3 times the size of the width-over-length ratio of a first transistor pair of the load.

13. (Previously Presented) The device according to claim 12, wherein the width of the transistors of the amplifying means and the transistors of the second transistor pair is in the range of 2.5-125 μm, and the length of the transistors is in the range of 0.25-12.5 μm; the width and the length, respectively, of the transistors of the tail-current sources and the transistors of the first transistor pair of the load are in the range of 0.25-12. 5 μm.

14. (Previously Presented) The device according to claim 1, further comprising a voltage controlled oscillator (VCO) having an input terminal, the input terminal coupled to a noise source.

15. (Previously Presented) The device according to claim 1, further comprising a current controlled oscillator (CCO) having an input terminal, the input terminal coupled to a noise source.

16. (Previously Preserted)The device according to claim 1, wherein the input terminal for receiving a bias input is coupled to a noise source for generating intrinsic noise, the noise source comprising a noisy amplifier cell having amplifying means, a load coupled to the amplifying means and supply, and a tail-current source coupled to grounding means and to the amplifying means.

17. (Previously Presented) The device according to claim 1, further comprising an electronic apparatus for generating a random sequence.

18. (Previously Presented)The device according to claim 17, wherein the electronic apparatus is one from the group consisting of a mobile radio terminal, a pager, a communicator, an electronic organizer and a smartphone.

19. (Previously Presented) The device according to claim 17, wherein the electronic apparatus is a mobile telephone.

20. (Previously Presented) The device according to claim 1, the device being fabricated in an integrated circuit.

21. (Previously Presented) The device according to claim 10, wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source, and the width-over-length ratio of a second transistor pair of the load is at least 3 times the size of the width-over-length ratio of a first transistor pair of the load.

22. (Previously Presented) The device according to claim 21, wherein the width of the transistors of the amplifying means and the transistors of the second transistor pair is in the range of 2.5-125 μm, and the length of the transistors is in the range of 0.25-12. 5 μm; the width and the length, respectively, of the transistors of the tail-current sources and the transistors of the first transistor pair of the load are in the range of 0. 25-12.5 μm.